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(54) Method and apparatus for processing a received wireless data signal.

(57) A local area network (10) utilizes a wireless transmission link and has network stations (12) each having two differently polarized antennas (14, 16). Data transmission utilizes a spread spectrum code and in the receiver, correlator outputs are utilized in an integrator and registers circuit (54) to provide correlator output sample values integrated over a plurality of symbol intervals. These values are stored in registers (156) the contents of which are utilized to determine a peak value and a total value which are applied to a spike quality determination circuit (78) including a look-up table (200). The resultant spike quality output value represents the quality of the received signal and is utilized for carrier detection and for antenna selection.

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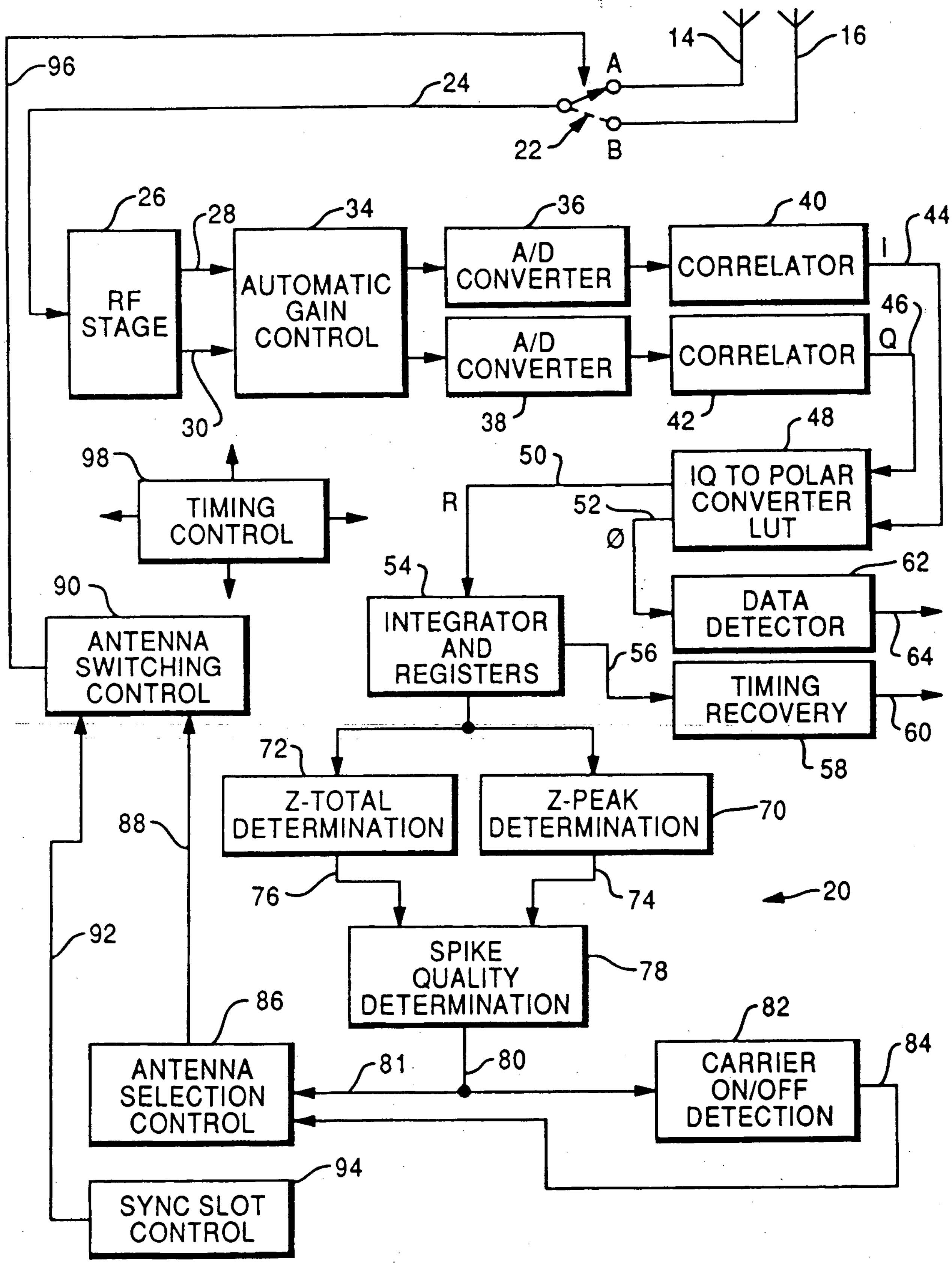
FIG. 2



96
24
14
16
A
B
22
26
28
34
36
40
44
RF STAGE
AUTOMATIC GAIN CONTROL
A/D CONVERTER
CORRELATOR
I
46
Q
A/D CONVERTER
CORRELATOR
30
38
42
48
98
TIMING CONTROL
50
IQ TO POLAR CONVERTER LUT
R
52
Ø
90
54
62
ANTENNA SWITCHING CONTROL
INTEGRATOR AND REGISTERS
DATA DETECTOR
56
64
TIMING RECOVERY
60
58
72
Z-TOTAL DETERMINATION
Z-PEAK DETERMINATION
70
88
76
74
20
92
SPIKE QUALITY DETERMINATION
78
86
82
81
80
84
ANTENNA SELECTION CONTROL
CARRIER ON/OFF DETECTION
94
SYNC SLOT CONTROL

This invention relates to the detection of received signal quality in a wireless data transmission system.

The invention has a particular application to wireless local area networks (LANs), and can be utilized for carrier detection and, in a multiple-antenna diversity system, for antenna selection.

Local area networks wherein a plurality of network stations are interconnected by cabling have become widely known and utilized. However, LANs using wired connections have the disadvantage that extensive cabling is required to interconnect the stations. The provision of such cabling is generally inconvenient, and gives rise to inflexibility if it is desired to alter the physical location of the stations. It has been proposed to utilize a wireless radio link for LANs. However, certain problems are associated with the use of a radio transmission link, particularly for LANs in an indoor environment. One such problem is multipath fading. The use of spread spectrum communication techniques alleviates the problems associated with multipath fading.

It is an object of the present invention to provide a method and apparatus for processing an encoded data signal transmitted over a wireless communication channel, whereby the received signal quality may be readily determined for a large range of receive levels.

Therefore, according to one aspect of the present invention, there is provided, in apparatus for receiving a signal representing data symbols encoded in a spread spectrum code, and transmitted over a wireless communication channel, a method for processing the received signal, characterized by the steps of: converting the received signal to a digital representation; correlating said digital representation to provide a plurality of signal samples; averaging said signal samples; determining a peak value and a total value for the averaged signal samples; and determining a spike quality value based on the ratio of said peak value and said total value.

According to another aspect of the present invention, there is provided apparatus for receiving data symbols encoded in a spread spectrum code and transmitted over a wireless channel, characterized by analog-to-digital conversion means adapted to provide a digital representation of a received signal, correlator means coupled to said analog-to-digital conversion means and adapted to provide a plurality of signal samples, integrator and storage register means including a plurality of storage registers adapted to store integrated representations of said signal samples, peak determining means adapted to determine the maximum value stored in said storage registers, total value determining means adapted to determine the total value of the values stored in said storage registers, and spike quality determining means adapted to provide a quality value signal representative of the quality of said received signal, in dependence on the ratio of said maximum value and said total value.

It will be appreciated that in a method and apparatus according to the invention, since the spike quality value is dependent on the ratio of peak and total values, the spike quality determination is largely independent of the received signal level, and hence such value will be satisfactorily determined for a large range of receive levels.

A further advantage of the invention is that a fast and reliable carrier detection may be achieved. This is important, for example in an application to a wireless LAN, in assisting in the achievement of a high throughput performance. Yet another advantage, in a system where a plurality of antennas is utilized, is that a fast and reliable antenna selection may be achieved, thereby assisting in the reliability of data transmission in the system.

A preferred embodiment of the present invention will now be described by way of example, with reference to the accompanying drawings, in which:-

Fig. 1 is a diagram of a radio LAN;

Fig. 2 is a block diagram of a portion of a transceiver section of a LAN network station;

Fig. 3 is a first embodiment of a correlator which may be used in the circuitry shown in Fig.2;

Fig. 4 is a second embodiment of a correlator which may be used in the circuitry shown in Fig. 2;

Fig. 5 is a detailed diagram of an integrator and registers block shown in Fig. 2;

Fig. 6 is a detailed diagram of the carrier on/off detection block shown in Fig. 2; and

Fig. 7A, 7B, and 7C are waveform diagrams helpful in understanding the operation of the present invention.

Referring first to Fig. 1, there is shown a radio local area network (radio LAN) 10 including a plurality N of stations 12, shown individually as 12-1 to 12-N. Each station has two antennas 14 and 16, which are polarized in different directions such as at right angles to each other, and are shown individually as 14-1 to 14-N and 16-1 to 16-N.

Communication among the stations 12 takes place on a single radio channel, and uses spread spectrum communication technology. In the indoor radio LAN of the preferred embodiment, the 902-928 MHz band is utilized. Another suitable frequency band lies around 2.5 GHz.

Referring now to Fig. 2, there are shown pertinent blocks of a transceiver circuit 20 included in a typical station 12. It should be understood that the station 12 includes additional circuits (not shown) such as a LAN controller device, a memory and a CPU, which are conventional devices, and because they are not of relevance to the present invention, they will not be described herein. In the preferred embodiment, information is transmitted using an 11-chip spread spectrum code based on quadrature modulation with two bits per symbol and

4DPSK (4 phase differential phase shift keying) coding.

The signals from the antennas 14 and 16 are passed via a switch 22 to a line 24 connected to an RF stage 26 which includes a 90 degree phase shifter (not shown) and provides in-phase and quadrature signals on respective lines 28 and 30, which are coupled to an automatic gain control circuit (AGC) 34. Respective in-phase and quadrature outputs from the AGC 34 are applied to respective analog-to-digital converters 36, 38 which provide digital outputs to respective correlators 40 and 42. The correlators 40 and 42 (to be described) are adapted to correlate their respective input signals in accordance with the spread spectrum code utilized in the transmission, and provide corresponding in-phase and quadrature spike output waveforms on lines 44 and 46. It should be understood that in the preferred embodiment, an 11-chip spread spectrum code is utilized, and each chip is sampled twice, whereby there are 22 samples per symbol. With these parameters, the correlators 40 and 42 provide output spike waveform having peaks after every 22 samples.

The in-phase and quadrature signals I and Q on the lines 44 and 46 are applied to an IQ to polar coordinate converter 48 which is implemented as a look-up table (LUT) and converts the in-phase and quadrature signals I and Q to polar signals R and Ø on output lines 50 and 52, where R represents a vector length or amplitude (modulus) and Ø represents a phase angle. The R signal on the line 50 is applied to an integrator and registers circuit 54 (to be described) which has an output 56 connected to a timing recovery circuit 58 which provides recovered timing signals on a line 60. The Ø signal on the line 52 is applied to a data detector circuit 62 which provides recovered data signals on a line 64.

An output of the integrator and registers circuit 54, which includes a plurality of Z-registers, is applied to a Z-peak determination circuit 70 and a Z-total determination circuit 72, which operate, in a manner to be described, on the contents of the registers included in the circuit 54, to provide a Z-peak value on a line 74 and a Z-total value on a line 76. The lines 74 and 76 are connected to a spike quality determination circuit 78 (to be described), which provides a spike quality value signal on a line 80. The line 80 is connected to a carrier on/off detection circuit 82 which provides an output over a line 84 to an antenna selection control circuit 86. The line 80 is also connected directly to the antenna selection and control circuit 86 over a line 81. The antenna selection and control circuit 86 provides an output over a line 88 to an antenna switching control circuit 90, which also receives an input over a line 92 from a sync slot control circuit 94. The antenna switching control circuit 90 provides an output over a line 96 to control the operation of the switch 22.

The circuit 20 includes a timing control circuit 98 which provides appropriate timing signals, where required, to the blocks shown in the drawing. However, to avoid complications in the drawing, the individual connections from the timing control circuit 98 to the individual blocks are not shown in Fig. 2.

Referring now to Fig. 3, there is shown a first embodiment of a correlator 100 which may be utilized for the correlator 40 or 42 shown in Fig. 2. The correlator 100 is in the form of a finite impulse response (FIR) filter having coefficients C_0, C_1, C_2, ..., C_{21}, which have the values +1 or -1 stored as values in a register 102. It should be understood that the spreading code used for the spread spectrum code of length 11 utilized in the preferred embodiment is:

+1, +1, +1, -1, -1, -1, +1, -1, -1, +1, -1.

Since the preferred embodiment operates with an oversampling factor of 2, the correlator has 22 coefficients, which have the values shown in the register 102.

The correlator input signal is applied over an input lead 104 to a 22-stage shift register 106, the stages of which successively store the input sample values S_K, S_{K-1}, ..., S_{K-21}. The outputs of the shift register stages, together with the corresponding coefficient values from the register 102 are applied to multipliers 108, the outputs of which are connected to an adder 110 which provides the correlation output signal on an output lead 112.

Referring to Fig. 4, there is shown an alternative embodiment of a correlator 120 which may be utilized for the correlator 40 or 42 shown in Fig. 2. The correlator 120 includes an input line 122 coupled to a shift register 124, the stages of which store successive sample values S_K, S_{K-1}, ..., S_{K-21}. The shift register stages are connected to an adder 126 or to an adder 128 according as the relevant coefficient value is +1 or -1. The outputs of the adders 126, 128 are connected as positive and negative, respectively, to an adder 130, which provides the correlator output signal on an output lead 132.

It will be appreciated that the +1 and -1 coefficient values used in the correlators shown in Figs. 3 and 4 enable a simple implementation to be achieved.

Referring now to Fig. 5, there is shown a more detailed diagram of the integrator and registers circuit 54, the Z-peak and Z-total determination circuits 70 and 72 and the spike quality determination circuit 78, shown as blocks in Fig. 2. In connection with Fig. 5, it should be understood that the short transverse lines which cross certain of the interconnecting leads indicate the number of bit-carrying conductors in the associated leads.

The 5-bit input line 50 is connected to a leaky integrator circuit 140 which includes an adder 142, a delay circuit 144, and a multiplier 146. The output of the adder 142 is connected to the input of the multiplexer circuit

144, the output of which is coupled via a feedback line 148 to a positive input of the adder 142, and via a line 150 to the multiplier 146, which has a constant 1/32 value applied thereto. The output of the adder 146 is connected over a line 152 to a negative input of the adder 142. The input line 50 is connected to a positive input of the adder 142. The multiplexer circuit 144 is also connected over a bidirectional 10-bit line 154 to a block of 22 registers 156, shown individually as registers 156-1 to 156-22. Outputs of the registers 156 are connected over a 10-bit line 158 to a bit deletion circuit 160, which deletes the two least significant bits and provides an 8-bit output on an 8-bit line 162. The manner of processing the multiplexer 144 and the registers 156-1 to 156-22 gives an effective delay of 22 sample intervals (one symbol period) between the adder 142 and lines 148 and 150. The multiplexer 144 is operated under the control of the timing control circuit 98 (Fig. 2).

The line 162 (Fig. 5) is connected to an input of the Z-peak determination circuit 70 and to an input of the Z-total determination circuit 72, which will now be described. The line 162 is connected to the input of an adder 170 which has an output connected to the input of a delay circuit 172, the output of which is connected via a feedback line 174 to a second input of the adder 170. The adder 170 operates only during 22 samples of the symbol on the line 162. The adder 170 effects summation, with overflow protection at a value of 2047, that is, the adder 170 has a maximum value of 2047. The output of the delay circuit 172 is also connected to a bit deletion circuit 176, which deletes the two least significant bits to provide a 9-bit output, the 9-bit output line 76 representing the Z-total value. The line 162 is also connected to the Z-peak determination circuit 70, which selects the maximum of the signals on the line 162 during 22 sample intervals (one symbol period).

The 8-bit line 74 (Z-peak value) and the 9-bit line 76 (Z-total value) are applied as inputs to the spike quality determination circuit 78. The 8-bit line 74 is connected to the input of a shifter circuit 190, and the 9-bit line 76 is connected to the input of a shifter circuit 192. The shifter circuits 190 and 192 are interconnected by a control line 194. The shifter circuits 190 and 192 effect multiplications by left shifting their contents and are arranged to operate such that they are shifted together by 0, 1, 2, 3 or 4 bit positions, until the most significant 1 bit in the Z-peak or Z-total value, as the case may be, is in the leftmost position. The 4-bit output of the shifter circuit 190 on the 4-bit line 196 and the 5-bit output of the shifter circuit 192 on the 5-bit line 198 are applied as address signals to address a spike quality look-up table (LUT) 200. The arrangement of the spike quality look-up table 200 is shown in Table 1. In Table 1, the horizontal values 0-15 represent Z-peak values, the vertical values 0-31 represent Z-total values and the table entries having values from 0 to 15 represent spike quality (SQ) values, with the value 15 representing the best spike quality and the value 0 representing the worst spike quality (no signal received).

TABLE 1

PEAK	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
TOTAL																
31	0	0	0	0	0	0	0	0	0	0	0	0	1	2	4	7
30	0	0	0	0	0	0	0	0	0	0	0	0	1	3	6	7
29	0	0	0	0	0	0	0	0	0	0	0	1	2	4	7	8
28	0	0	0	0	0	0	0	0	0	0	0	1	3	5	7	8
27	0	0	0	0	0	0	0	0	0	0	0	2	4	6	8	9
26	0	0	0	0	0	0	0	0	0	0	1	2	5	7	9	10
25	0	0	0	0	0	0	0	0	0	0	1	3	6	7	10	10
24	0	0	0	0	0	0	0	0	0	0	2	4	7	8	10	11
23	0	0	0	0	0	0	0	0	0	1	2	5	8	9	11	11
22	0	0	0	0	0	0	0	0	0	1	3	6	9	10	12	12
21	0	0	0	0	0	0	0	0	1	2	4	7	9	10	12	13
20	0	0	0	0	0	0	0	0	1	3	5	8	10	11	13	14
19	0	0	0	0	0	0	0	0	2	4	6	9	11	12	13	14
18	0	0	0	0	0	0	0	1	2	5	7	9	11	12	14	14
17	0	0	0	0	0	0	0	1	3	6	8	10	12	13	14	14
16	0	0	0	0	0	0	0	2	4	7	9	11	13	14	14	14
15	0	0	0	0	0	0	1	2	5	8	10	12	13	14	14	15
14	0	0	0	0	0	0	1	3	6	9	11	13	14	14	15	15
13	0	0	0	0	0	0	2	3	7	10	12	13	14	15	15	15
12	0	0	0	0	0	0	2	4	9	11	13	14	14	15	15	15
11	0	0	0	0	0	1	3	5	10	12	14	14	15	15	15	15
10	0	0	0	0	0	1	3	6	12	14	14	15	15	15	15	15
9	0	0	0	0	0	2	4	7	14	14	15	15	15	15	15	15
8	0	0	0	0	1	2	5	8	14	15	15	15	15	15	15	15
7	0	0	0	0	1	3	6	9	15	15	15	15	15	15	15	15
6	0	0	0	0	2	3	7	10	15	15	15	15	15	15	15	15
5	0	0	0	1	2	4	8	12	15	15	15	15	15	15	15	15
4	0	0	1	1	3	5	9	13	15	15	15	15	15	15	15	15
3	0	0	1	2	3	6	10	15	15	15	15	15	15	15	15	15
2	0	0	2	3	4	7	11	15	15	15	15	15	15	15	15	15
1	0	1	2	3	5	8	13	15	15	15	15	15	15	15	15	15
0	0	1	3	4	6	9	15	15	15	15	15	15	15	15	15	15
PEAK	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

The 4-bit output of the spike quality look-up table 200, in accordance with Table 1, is applied over the 4-bit output line 80. It will be appreciated that a spike quality value of 15 indicates very good signal reception quality whereas a spike quality value of 0 indicates that no signal is received. An intermediate spike quality value indicates an intermediate signal quality reception condition.

The circuitry shown in Fig. 5 is operative only when the transceiver 20 is in the receive mode, and is processed partially per sample, which in the preferred embodiment is at a 22 MHz rate, and partially per symbol which, in the preferred embodiment, is at a 1 MHz rate. This receive mode processing starts after 36 symbol periods from the beginning of an antenna slot interval. It should be understood that when no carrier signal is detected by the transceiver 20, the antenna switching control circuit 90 (Fig 2) causes the switch 22 to alternate between a state A slot interval (antenna 14 operative) and a state B slot interval (antenna 16 operative). Each antenna slot interval has a duration of 40 symbol periods. When a carrier signal is detected, the antenna switch-

ing control circuit 90 is further operative for a few antenna slot intervals, as will be explained hereinbelow, during which the Fig. 5 circuitry provides spike quality values for the respective states A and B, whereby whichever of state A and state B has the better determined spike quality is switched to or maintained during the reception of the received data frame. During transmission by the transceiver 20, the state A is always operative.

With the above in mind, the processing of the Fig. 5 circuitry will now be described. During the time that the antenna switching control circuit 90 causes alternate switching between states A and B, the Fig. 5 circuitry is controlled, under the timing control circuit 98 (Fig. 2) to be processed only during the last 4 symbol periods (corresponding to 4x22=88 samples) of the slots, which, as mentioned, are each 40 symbol periods long. During these 4 symbol periods, which commence after the expiration of 36 symbol periods from the commencement of each antenna slot interval, the leaky integrator circuit 140 (Fig. 5) and the registers 156 are processed. This processing effects that successive samples R are added to the contents of the registers 156-1 to 156-22, respectively, to calculate the changing average of the rectified spike waveform. The leaky integrator circuit 140 adds the sample value R to $^{31}/32$ times the previous register 156-2 value Z_1 and stores the new Z_1 value in the register 156-1; then adds the sample value R_{K+1} to $^{31}/32$ times the previous register 156-2 value Z_2 and stores the new Z_2 value in the register 156-2; and proceeds in this manner to successively process the remaining registers 156-3 to 156-22. After processing the register 156-22, the leaky integrator circuit 140 reverts to processing the register 156-1 again, and proceeds in this manner as long as it is operative. More precisely, during a period of 4 symbol intervals just before the end of the antenna slot, the correlator output samples are rectified (modulus value) and added to the contents of 22 registers 156 as follows:

The values of the 1st, 23rd, 45th, and 67th sample are added to Register 1.

The values of the 2nd, 24th, 46th, and 68th sample are added to Register 2.

The values of the 3rd, 25th, 47th, and 69th sample are added to Register 3.

The values of the 22nd, 44th, 66th, and 88th sample are added to Register 22.

Thus the contents of the Registers 1 through 22 corresponds to 22 samples of a signal. This signal is 4 times the average of the rectified spike waveform.

At the end of each 4 symbol period, that is, at the end of the relevant antenna slot interval, the Z-peak determination circuit 70 and the Z-total determination circuit 72 are each processed once, whereby a 4-bit spike quality value output signal is provided on the output line 80. Thus, in a relevant antenna slot interval, the spike quality value signal is derived once at the end of the interval, based on the 22 register values Z found-by integration during 4 symbol periods.

Summarizing, it will be appreciated that, after processing, the contents of the 22 registers 156-1 to 156-22 correspond to 22 samples of a signal. This signal is 4 times the average of a rectified spike waveform. The register with the highest value provides the Z-peak value determined by the Z-peak determination circuit 70. In the Z-total determination circuit 72 the contents of the 22 registers 156 are summed to provide the Z-total value. As is evident from Table 1, the higher Z-peak is, compared to Z-total, that is, the ratio of Z-peak to Z-total, the higher is the spike quality value. As will be explained in more detail hereinafter, a carrier ON detection signal is provided by the carrier on/off detection circuit 82 (Fig. 1) at the end of an antenna slot interval when the spike quality value based on these 4 symbols is above a predetermined threshold. If the correlation effected by the correlators 40 and 42 (Fig. 2) provides a good spike waveform during successive symbols, then the Z-peak value is relatively high and the spike quality value will be above the threshold.

Referring now to Fig. 6, there is shown an embodiment of the carrier on/off detection circuit 82 (Fig. 1). The spike quality value signal is applied via the line 80 to a switch 210 which has two interconnected switch arms 212 and 214. Of course, in a practical implementation, the switch 210 is an electronic switch. The switch arm 212 contacts either a first terminal 216 which is connected to the input of a comparator 218, or a second terminal 220 which is unconnected. The switch arm 214 contacts either a first terminal 222 which is unconnected, an a second terminal 224, which is connected to an input of a comparator 226. The output of the comparator 218 is connected to an input of an OR gate 228. The output of the OR gate 228 is connected over a line 230 to an input of a carrier on/off mode control circuit 232, and via a line 231 to a control input 234 of the switch 210. The comparator 226 has an output connected over a line 240 to an input of the carrier on/off mode control circuit 232, and over a line 242 to a further control input 244 of the switch 210.

It will be appreciated that the carrier an/off detection circuit 82 has two different thresholds. Initially, the arms 212 and 214 of the switch 210 are in their lower, dashed line positions, contacting the terminals 220 and 224, respectively. If a spike quality value of 3 or more is detached, the comparator 226 is operative to provide an output to the mode control circuit 232 which provides a carrier detect signal on the output line 84. Also, via the line 242, the switch 210 is operated to the position shown wherein the arm 212 contacts the terminal 216, and the arm 214 contacts the terminal 222. If during a transmission, the spike quality becomes 0, then the comparator 218 is operative via the OR gate 228 to provide an input signal to the carrier on/off mode control circuit 232 indicating that the carrier is no longer present. Of course, this takes place at a time interval after the dis-

appearance of the spike waveform, because of the effect of the integration provided by the leaky integrator circuit 140 (Fig. 5). Normally, at the end of a transmission, a special postamble character is detected and operates the OR gate 228 over a line 250.

It will be appreciated that a very reliable carrier ON detection is achieved under many types of signal impairment, by virtue of the integration over a plurality, 4 in the preferred embodiment, of symbol periods.

The utilization of the spike quality value for antenna selection will now be described, with reference to Figs. 7A to 7C, and Table 2. In each of Figs. 7A to 7C, the first waveform (1) represents the state of the antenna switch 22 (A or B). The second waveform (2) represents carrier activity and the third waveform (3) represents the carrier on/off signal provided by the detection circuit 82 (Fig. 2).

The following Table 2 is a state table for antenna selection control circuit 86, Fig. 2, after carrier detection has taken place.

TABLE 2

Occurrence of Spike Quality (SQ) values during 2 or 3 antenna slots	Action
(a) 1st SQ better than 2nd SQ	switch definitively to 1 SQ antenna
(b) 1st SQ worse than 2nd SQ	wait for SQ 3rd slot
(b1) 2nd SQ better than 3rd SQ	switch definitively to 2nd SQ antenna
(b2) 2nd SQ worse than 3rd SQ	switch definitively to 1st (3rd) SQ antenna

The utilization of spike quality values for two or three antenna slot intervals guarantees an appropriate selection for all situations. It should be understood that the LAN 10, Fig. 1, has a synchronization provision whereby the sync slot control circuit 94 (Fig. 2) in each station 12 provides for synchronization among the stations by ensuring that the antenna slot intervals are synchronized for all the stations 12. Also, each transmission is controlled to commence at the beginning of an antenna slot. Thus, when a carrier signal is present from the beginning of an antenna slot, the automatic gain control in the receiver stage of the transceiver will be stabilized by the end of that antenna slot, and a clean spike waveform will be provided, such that the spike quality value will be above the threshold (of value 3 in the preferred embodiment) for carrier detection. Referring to Table 2, situation (a), and to Fig. 7A, if the first spike quality value detected is better than the second spike value, the selection control circuit 86 provides for switching to the first antenna. This is illustrated by way of example in Fig. 7A by a switching to state B whereby antenna 16 is utilized for the data reception.

On the other hand, if the first spike quality is worse than the second spike quality, the control circuit 86 waits for the third antenna slot and utilizes the spike quality value thereof for further comparisons, see situation (b) in Table 2. In situation (b1), it is determined that the second spike quality is better than the third spike quality. In this situation, the control circuits 86 causes switching for data reception to the antenna providing the second spike quality value, see Fig. 7B, where there is illustrated switching to state A, corresponding to antenna 14, for data reception. In situation (b2), it is determined that the second spike quality is worse than the third spike quality. There is no further antenna switching, see Fig. 7C, from which it is seen that state B is maintained for data reception.

It will be appreciated that a situation may arise wherein the aforementioned station synchronization has deteriorated, such that a carrier signal arises at the middle of an antenna slot, instead of at the beginning thereof. In this situation, the automatic gain control in the receiver will not be stabilized at the end of an antenna slot. Thus, the first spike quality value detected will refer to the absence of sufficiently good receive condition. However, at subsequent antenna slots appropriate spike quality values will be determined at the end of such slots.

In these circumstance, situation (b) in Table 2 is pertinent.

The data frames utilized for data transmission in the preferred embodiment each contain a preamble portion which includes a plurality of training sequence symbols, corresponding to a total duration of five antenna slots. Within the duration of four of these slots, carrier detection and a correct antenna selection are guaranteed by the above-described procedures. The fifth antenna slot interval can then be utilized for the adjustment of other receive functions.

After carrier detection and antenna selection (when alternate switching between states A and B has been terminated), the Fig. 5 circuitry and the timing control circuit 98 are processed for each symbol interval and the contents of the registers 156-1 to 156-22 correspond to 22 samples of a signal waveform. This signal waveform is 32 times the moving average of the rectified spike waveform. If the spike waveform disappears but no post-amble character has been received, the spike quality (SQ) becomes zero, which results in carrier OFF detection.

It will be appreciated from the description of the preferred embodiment that the processing of the spike quality is independent of the receive level. Therefore the spike quality will function for a large range of receive levels. The spike quality depends on the quality of the spike waveform received from the ratio of Z-peak and Z-total. The ratio between Z-peak and Z-total is dependent on the relation between signal level and the levels of noise, interference and channel distortion effects. This ratio is thus relevant for the reliability of data transmission. The spike quality value is based on this ratio and is therefore an appropriate reference to select the best antenna. Carrier ON detection is made when a carrier signal is received sufficiently satisfactorily. The spike quality approach ensures for carrier ON detection a high reliability under all kinds of impairments. This reliability is possible by carrier ON detection through the spike quality criterion based on integration during only 4 symbol periods. The reliability of carrier ON detection within 4 symbols after AGC stabilization is important for throughput performance under various impairments. Also, an economy of circuitry is achieved since the integrator and registers circuit 54, Fig. 2, can be additionally employed for timing recovery.

A further advantage of the described embodiment is that two antennas are provided at each station, together with a selection means which selects one of the two antennas at the beginning of the reception of a data frame. This provides an improvement over the application of a single antenna since the probability that both antennas are subject to unacceptable fading or disturbance conditions is very much lower than for a single antenna. The described embodiment provides a fast and reliable antenna selection based on an appropriate quality measurement for the reliability of data transmission which depends on relevant receive conditions such as signal to noise ratio, signal to interference ratio and channel distortion.

Modifications are possible within the scope of the appended claims. Thus, although a spread spectrum code having 11 chips and employing 2 samples per chip has been described, it will be appreciated that a spread spectrum code having a different number of chips and/or a different number of samples per chip could be employed. Also, forms of modulation could be employed other than the described 4DPSK coding. Thus, for a spread spectrum code with one bit per symbol, only a single correlator need be utilized, having an output connected directly to an integrator and registers circuit, without the need for a coordinate conversion (IQ to polar) block. In another modification, the two antennas may be directed in different orientation directions instead of being polarized in different directions. Futhermore, the wireless transmission link employing a spread spectrum code may utilize transmission frequencies greater than radio frequencies, that is, greater than 3000 GHz. For such frequencies, of course, a type of antenna different from that used for radic frequencies would be employed.

Claims

1. In apparatus for receiving a signal representing data symbols encoded in a spread spectrum code, and transmitted over a wireless communication channel, a method for processing the received signal, characterized by the steps of: converting the received signal to a digital representation; correlating said digital representation to provide a plurality of signal samples; averaging said signal samples; determining a peak value and a total value for the averaged signal samples; and determining a spike quality value based on the ratio of said peak value and said total value.

2. A method according to claim 1, characterized by the steps of transmitting said data symbols using a carrier signal on said wireless communication channel, and utilizing said spike quality value to detect the reception of said carrier signal.

3. A method according to claim 1, characterized by the steps of providing a plurality of antennas (14,16); and utilizing said spike quality value to select one of said plurality of antennas (14,16) for signal reception.

4. Apparatus for receiving data symbols encoded in a spread spectrum code and transmitted over a wireless channel, characterized by analog-to-digital conversion means (36,38) adapted to provide a digital representation of a received signal, correlator means (40,42,48) coupled to said analog-to-digital conversion means (36,38) and adapted to provide a plurality of signal samples, integrator and storage register means (54) including a plurality of storage registers (156) adapted to store integrated representations of said signal samples, peak determining means (70) adapted to determine the maximum value stored in said storage registers (156), total value determining means (72) adapted to determine the total value of the values stored in said storage registers (156), and spike quality determining means (78) adapted to provide a quality value signal representative of the quality of said received signal, in dependence on the ratio of said maximum value and said total value.

5. Apparatus according to claim 4, characterized by carrier detection means (82) responsive to said quality value to provide a carrier detect signal.

6. A apparatus according to claim 4, characterized in that said spike quality determining means (78) includes a look-up table (200) addressable by address signals dependent on said maximum value and said total value.

7. Apparatus according to any one of claim 4 to 6, characterized in that said correlator means includes first and second correlators (40,42), corresponding to inphase and quadrature signal components, and conversion means (48) coupled to the outputs of said first and second correlators (40,42) and adapted to convert the output signals of said correlators (40,42) to an amplitude signal representation and phase angle signal representation, wherein said amplitude signal representation is applied to said integrator and storage register means (54).

8. Apparatus according to any one of claims 4 to 7, characterized in that said integrator and storage register means (54) includes a leaky integrator (140) adapted to receive said signal samples, and coupled to said plurality of storage registers (156).

9. Apparatus according to claim 7, characterized in that said carrier detection means (82) includes first threshold means (226) adapted to be operated in response to said quality value signal exceeding a first predetermined value, and second threshold means (218) adapted to be operated in response to said quality value signal equalling a second predetermined value.

10. Apparatus according to any one of claims 4 to 9, characterized by first and second antennas (14,16), switching means (22) adapted to selectively render said first and second antennas (14,16) operative, and switching control means (86,90) adapted to operate said switching means for successive uniform antenna slot intervals.

11. Apparatus according to claim 10, characterized in that said first and second antennas (14,16) have different polarization directions.

12. Apparatus according to claim 10, characterized in that said first and second antennas (14,16) have different orientation directions.

13. Apparatus according to any one of claims 10 to 12, characterized in that said switching control means (86,90) is adapted to control the selection of said first or second antenna (14,16) in dependence on the relative quality values provided by said spike quality determining means (78) during successive antenna slot intervals in which said first and second antennas 14,16 are successively operative

14. Apparatus according to any one of claims 10 to 13, characterized in that said spike quality determining means (78) is operative for a predetermined number of symbol periods occurring at the end of an antenna slot interval.

FIG. 1

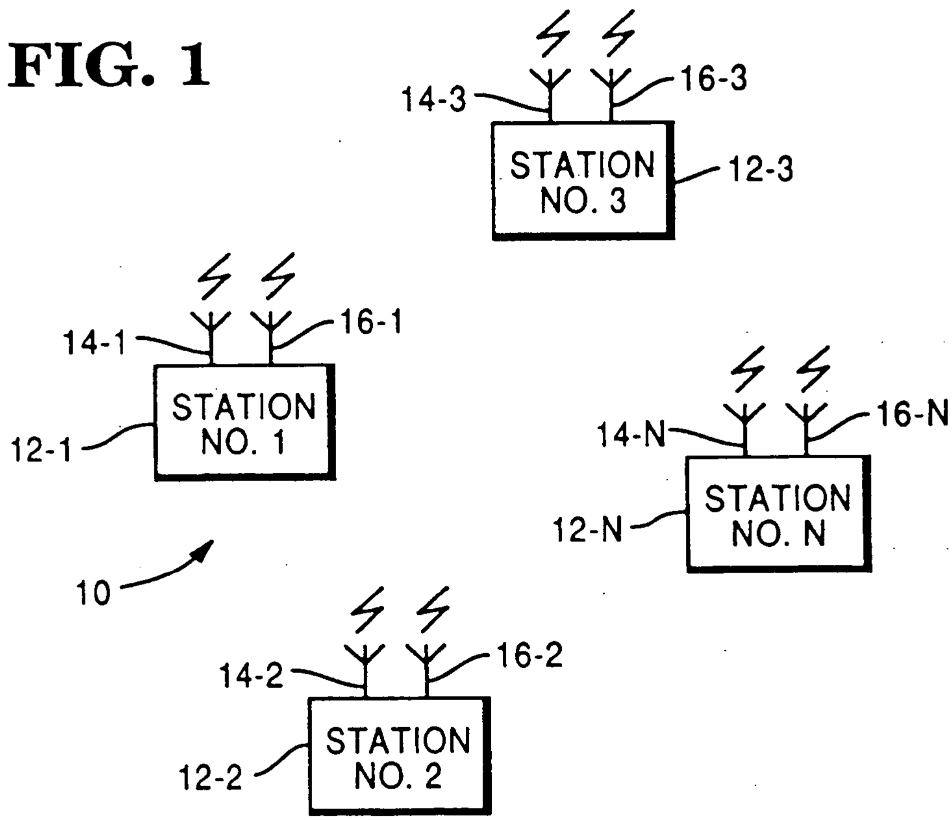

14-3
16-3
STATION NO. 3
12-3
14-1
16-1
STATION NO. 1
12-1
14-N
16-N
STATION NO. N
12-N
10
14-2
16-2
STATION NO. 2
12-2

FIG. 2

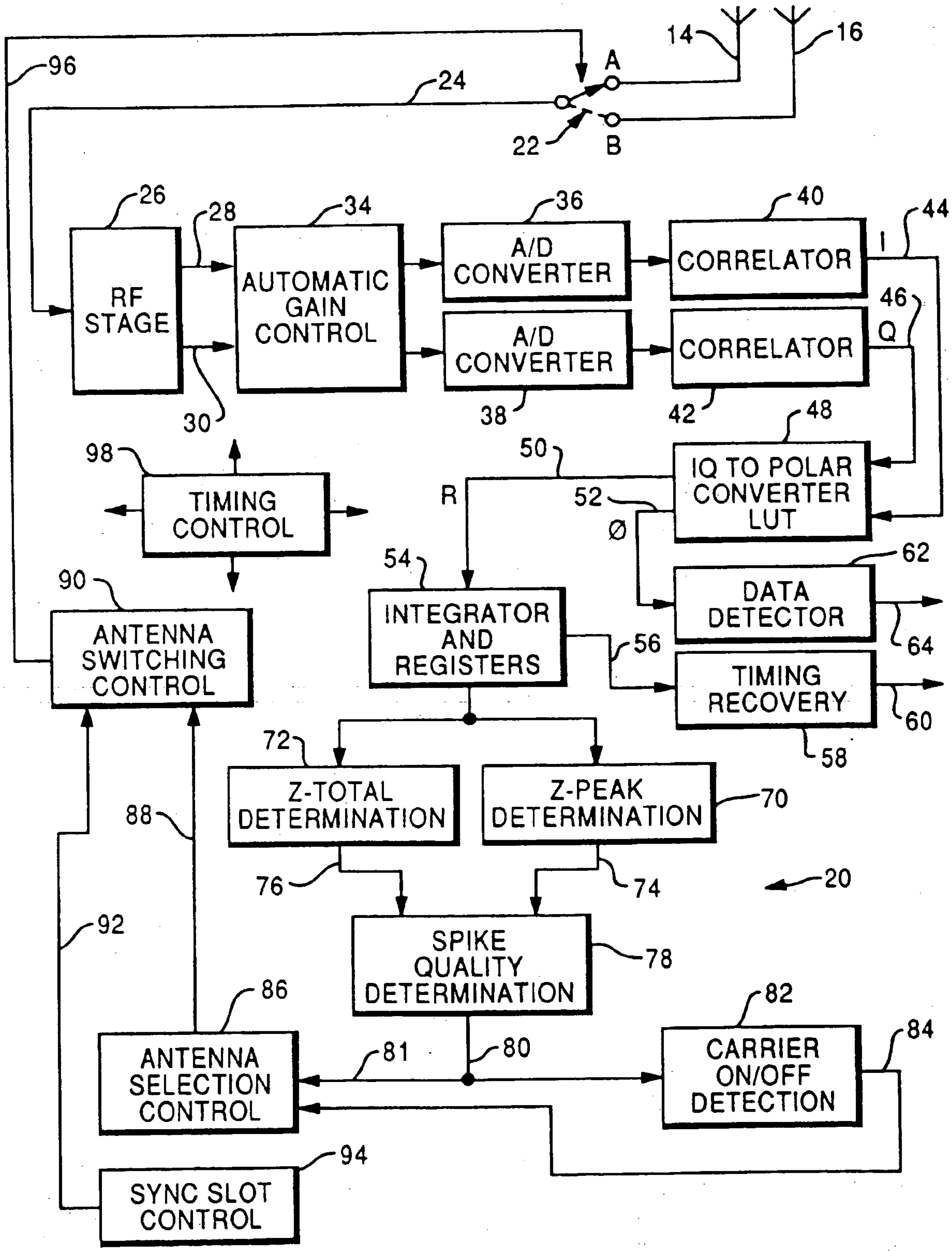

14
16
A
B
96
24
22
26
28
34
36
40
44
RF STAGE
AUTOMATIC GAIN CONTROL
A/D CONVERTER
CORRELATOR
I
46
Q
A/D CONVERTER
CORRELATOR
30
38
42
48
98
TIMING CONTROL
50
IQ TO POLAR CONVERTER LUT
R
52
Ø
62
54
90
DATA DETECTOR
64
ANTENNA SWITCHING CONTROL
INTEGRATOR AND REGISTERS
56
TIMING RECOVERY
60
58
72
Z-TOTAL DETERMINATION
Z-PEAK DETERMINATION
70
88
76
74
20
92
SPIKE QUALITY DETERMINATION
78
86
82
84
ANTENNA SELECTION CONTROL
81
80
CARRIER ON/OFF DETECTION
94
SYNC SLOT CONTROL

FIG. 3

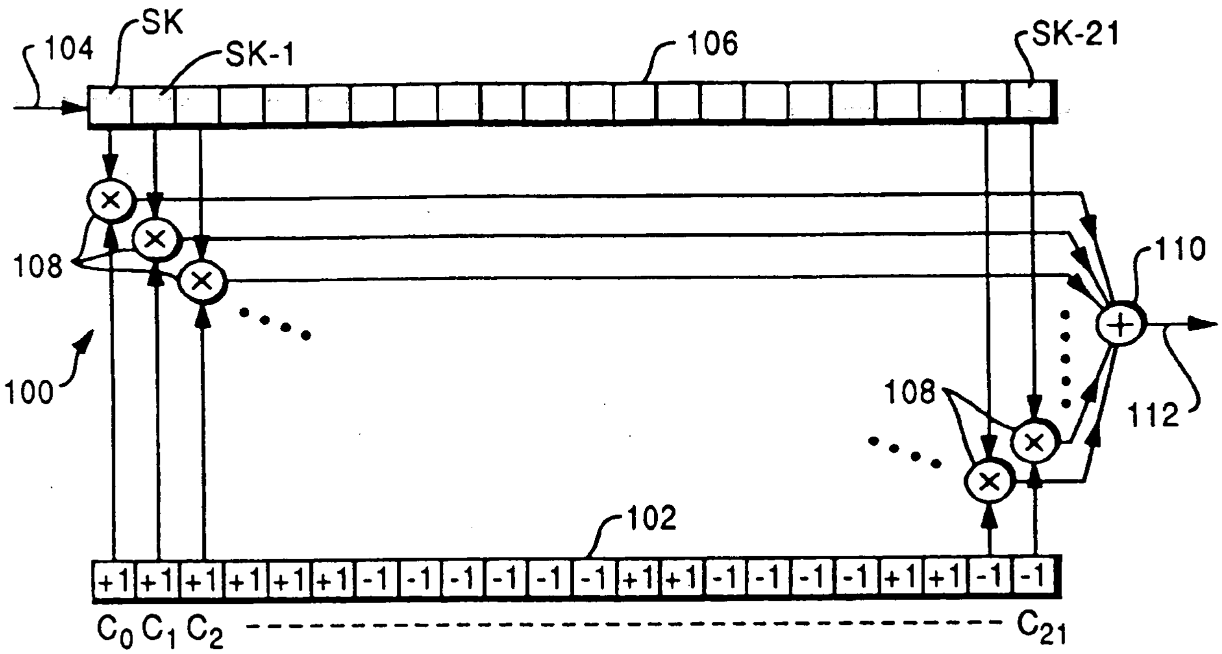

104
SK
SK-1
106
SK-21
108
110
100
112
108
102
+1 +1 +1 +1 +1 +1 -1 -1 -1 -1 -1 -1 +1 +1 -1 -1 -1 -1 +1 +1 -1 -1
C_0 C_1 C_2
C_{21}

FIG. 4

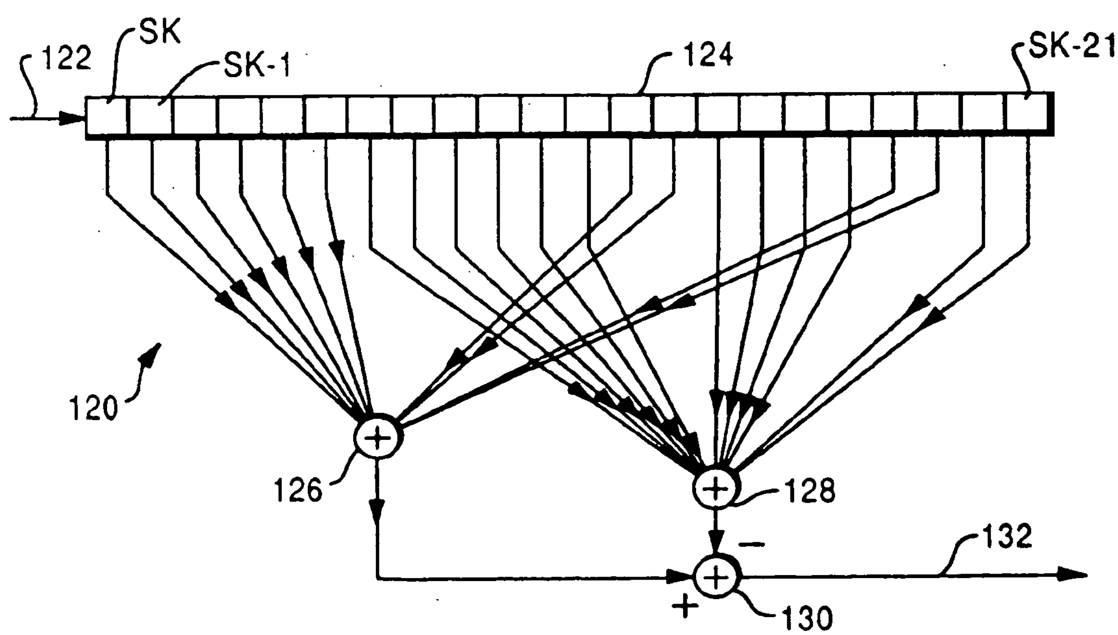

122
SK
SK-1
124
SK-21
120
126
128
-
132
+
130

FIG. 5

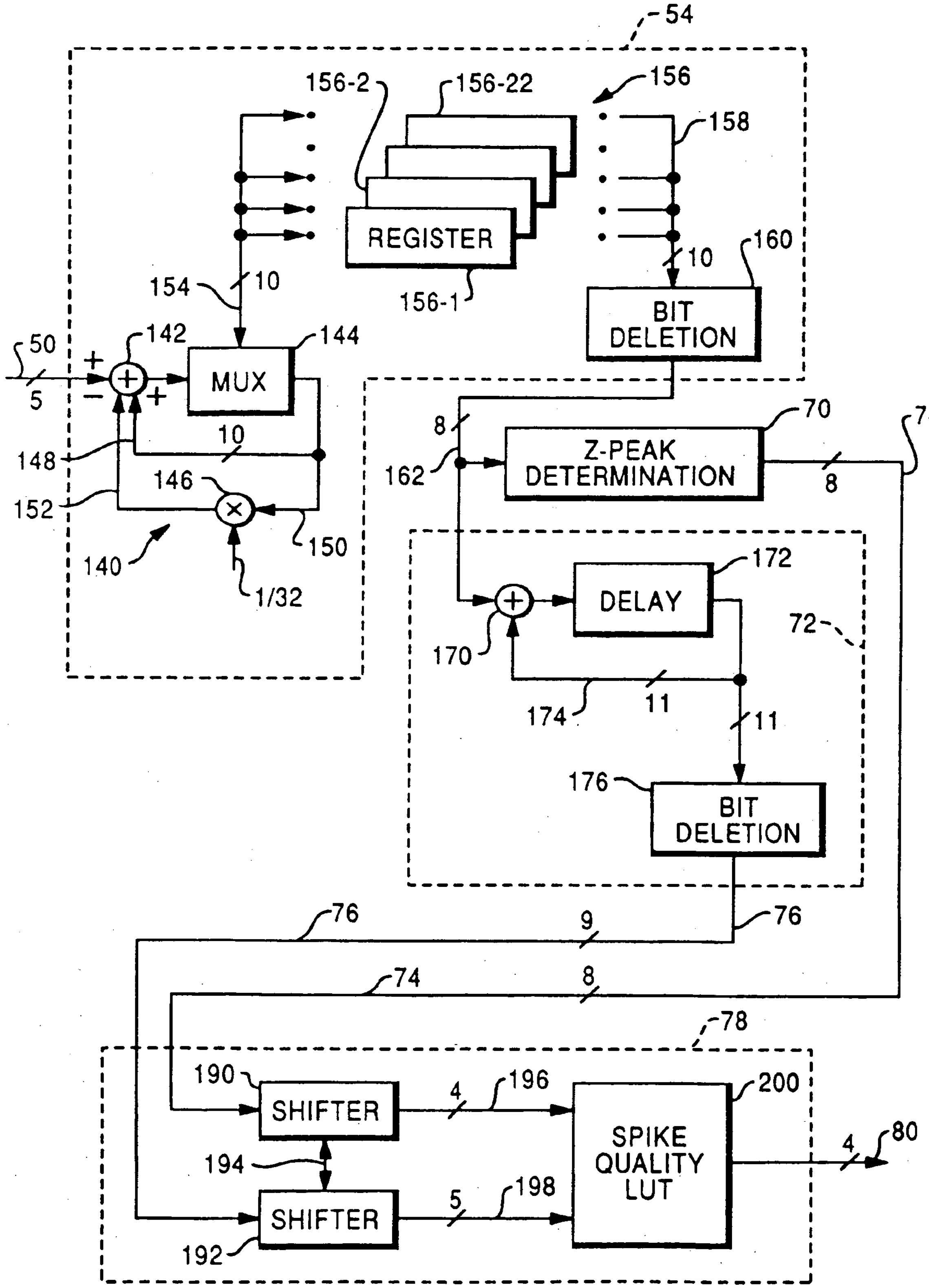

54
156-2
156-22
156
158
REGISTER
156-1
10
154
10
160
BIT DELETION
50
142
144
+
MUX
5
−
+
10
148
146
152
150
140
1/32
8
70
Z-PEAK DETERMINATION
74
162
8
172
DELAY
72
170
174
11
11
176
BIT DELETION
76
9
76
74
8
78
190
SHIFTER
4
196
200
SPIKE QUALITY LUT
194
4
80
SHIFTER
5
198
192

FIG. 6

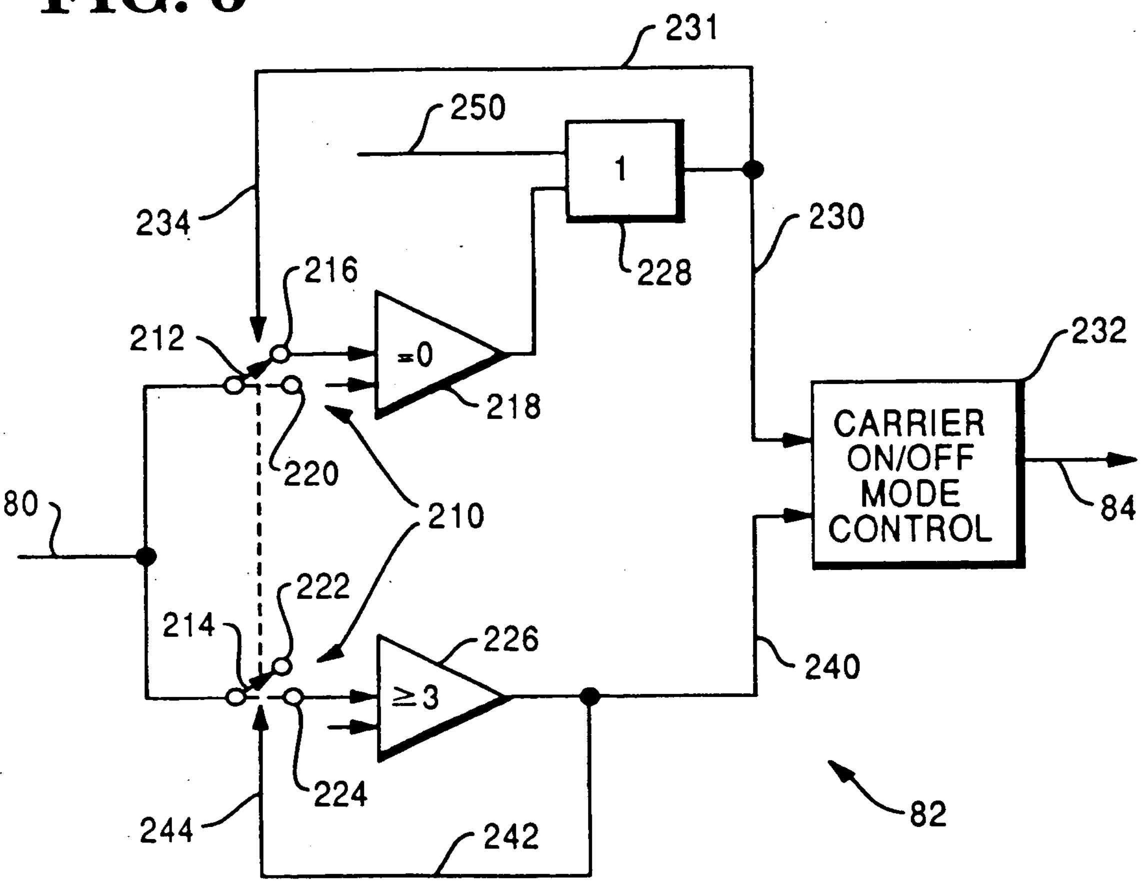

231
250
1
234
230
216
228
212
=0
232
218
CARRIER
ON/OFF
MODE
CONTROL
220
80
210
84
222
214
226
≥3
240
224
82
244
242

FIG. 7A

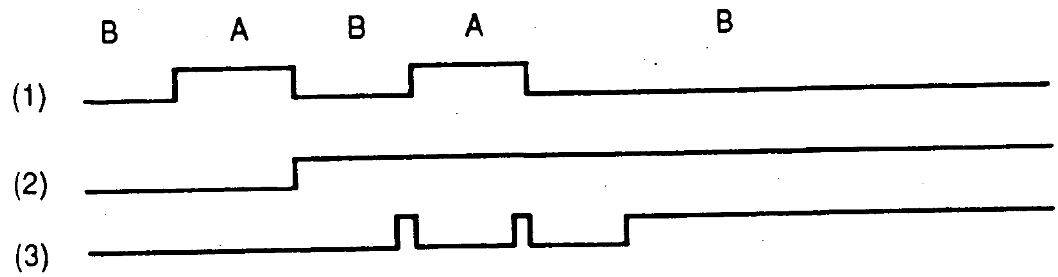


FIG. 7B

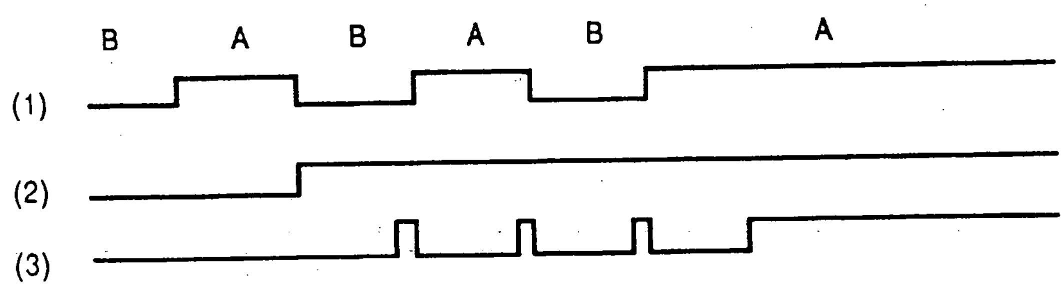


FIG. 7C